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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,342	LAHIRI ET AL.	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-19* is/are allowed.

6)☐ Claim(s) *1-10 and 20-27* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 have been presented for examination based on applicant's disclosure filed on 13 April 2001. Claims 1-10 and 20-27 have been rejected by the examiner. Claims 11 and 12 are objected to. Claims 13-19 have been allowed over the prior art of record.

Drawings

2. Applicant's drawings filed on 13 April 2001 have been approved by the examiner.

Claim interpretation

3. Applicant's are claiming limitations relating to a method and system for simulating the performance of a segmented cache memory of various sizes by applying data references to the simulated cache, storing the references in a trace buffer, calculating the number or "hits" or "misses" to the segments, and generating a performance estimate. Commercially available cache simulators that include many of these features, such as the "Cheetah" or "Pixie" programs, are well-known in the art and commonly used to experiment with and test different caching algorithms, decide on certain cache geometries, and predict cache performance. (See: Ravindran, page 115, para: 3, "Cheetah", Uhlig, table VII, for example)

The examiner has interpreted the term "operational data cache", recited in independent claims 1 and 20, to simply be the modeled cache geometries used by the cache simulator in determining the cache performance on an operational data

processing system. (specification page 2, line 23) The term "multi-segmented cache simulator" comprising simulated buffers, as recited in claim 13, is interpreted as specifically defined in applicants specification on page 9, lines 5-25, page 14, lines 12-27, and in Figs. 2 and 4a – 4b. (i.e. the multi-segments are the eight segments of cache simulator (200) designated as cache0-cache7 configured to hold 250,000 simulated buffers)

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-10 and 20-27 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,940,618 issued to Blandy et al.

Independent claim 1 is drawn to:

method of predicting cache performance by:
- storing data references applied to an operational data cache in a data processing environment;
- applying data references to cache simulator to simulate caches of different sizes, where cache simulator comprises multiple segments and each simulated cache comprises one or more segments;
- generating for each simulated cache an estimate of performance
- each application of data references to cache simulator causes "hit" in one of segments or "miss" of every segment.

Regarding independent claim 1: Blandy discloses a method and system for predicting and monitoring the performance of a cache memory using a cache simulator

(CL2-L28) where data (and code) is applied the cache simulator in a data processing environment (CL2-L29) so the performance of cache segments (CL2-L25) can be evaluated and improved. (Also see: Abstract, Summary, Figs. 4&5) Blandy teaches the elements of the claimed limitations of the present invention as follows:

- storing data references applied to an operational data cache in a data processing environment: Blandy discloses storing (CL5-L28) trace data collected from a processing environment as monitored segments (CL5-L19-26) representing operational data cache references (instruction cache and data cache accesses) that are to be applied to the cache simulator (CL5-L29). That is, the traced data collected the Blandy system represents operational data that is stored by the system and then applied to the input of cache simulator, as does the claimed invention.

- applying data references to cache simulator to simultaneously simulate caches of different sizes, where cache simulator comprises multiple segments and each simulated cache comprises one or more segments: Blandy discloses applying the stored (collected) data references (i.e. the instruction cache and data cache accesses) to the cache simulator as inputs (CL5-L30). Blandy also discloses simulating caches of different sizes (CL5-L53-54, CL5-L35). Blandy further discloses simulating more than one (multiple) cache segment (i.e. simulating both an instruction cache and a data cache) as part of the cache simulator (CL5-L19, CL5-L53). Therefore, Blandy discloses simultaneously simulating multiple cache segments. The examiner notes that commercially available cache simulators such as Cheetah (mentioned above) provide simulation and performance evaluation of multi-sized cache memory on more than one

cache segment (See: Abraham, page 12, para: 3, and Uhlig, table VII, for example). Blandy discloses using such a cache simulator embedded in a system for monitoring performance in an information handling system (see: CL5-L29-48).

- generating for each simulated cache an estimate of performance: Blandy discloses estimated performance results (CL5-L33, CL5-L48) from the simulated cache.

- each application of data references to cache simulator causes "hit" in one of segments or "miss" of every segment: Blandy discloses calculating the simulated cache "hit" and "miss" ratio (CL5-L30) for each simulated segment (CL3-L54-57) based on the applied data references (CL5-L26). Hence, Blandy teaches causing the "hits" and "misses" in the segments.

Per dependent claim 2: Blandy discloses the simulated cache geometry (size) to match the collected trace data representing the operational data cache (CL5-L52-55).

Per dependent claim 3: Blandy discloses evaluating the performance in an information handling system (CL2-L21) which the examiner interprets to include a database management system.

Per dependent claim 4: Blandy discloses receiving and storing operational cache data in a trace buffer (CL5-L27-28). Storing/discarding a data reference if the buffer is empty/full would be inherent part of the process of maintaining the trace buffer.

Per dependent claims 5 and 6: These claims include limitations relating to the storing and searching for data "identifiers" in the cache simulator buffers. The examiner asserts that this process would be necessarily inherent in the cache simulator disclosed

by Blandy in order to track and identify real time trace and simulation data. (see: Blandy CL5-L23)

Per dependent claims 7-10: These claims include limitations relating to incrementing the "hit and "miss" counter and updating data "identifiers" in the cache simulator buffers and calculating "hit and "miss" rates. The examiner again asserts that this process would be necessarily inherent in the cache simulator disclosed by Blandy in order to track and identify real time trace and simulation data and maintain the "hit and "miss" counters. (see: Blandy CL5-L29-45) The correction factor as recited in claim 10 would also be inherent since this process merely requires converting the initial estimates into final estimates (applicant's specification, page 13, line 13) which would again be a necessary part of calculating the "hit and "miss" rates.

Regarding independent claim 20: This claim merely claims the computer code and storage medium for the same limitations recited in independent claim 1 and is therefore rejected using same reasoning as previously cited above.

Regarding independent claim 21: Claim 21 includes limitations relating to computer readable storage medium and data structure for configuring the simulated caches. As previously cited above, Blandy discloses a software method and system for predicting and monitoring the performance of a cache memory using a cache simulator (CL2-L28) where data (and code) is applied the cache simulator in a data processing environment (CL2-L29) so the performance of cache segments (CL2-L25) can be evaluated and improved. (Also see: Abstract, Summary, Figs. 4&5) The method disclosed by Blandy includes a software data structure (Figs. 2a-2b) for simulating

caches of different sizes (CL5-L53). Hence, the computer readable storage for such features would be inherent. Blandy further discloses receiving and storing operational cache data in trace (simulated) buffers (CL5-L27-28). As also previously cited above, the data "identifiers" in the cache simulator buffers would be necessarily inherent in the cache simulator disclosed by Blandy in order to track and identify real time trace and simulation data (see: Blandy CL5-L23) as would incrementing the "hit and "miss" counters (see: Blandy CL5-L29-45).

Per dependent claim 22: Including and "identifier" at the head of the data structure list portion would also be necessarily inherent in order to track and identify real time trace and simulation data (see: Blandy CL5-L23).

Per independent claim 23: Claim 23 includes limitations relating to the system for simulating caches including the memory for data references, simulated buffers, and an engine for generating the data references. Blandy discloses limitations relating to data references, simulated buffers and generating the data references to the cache simulator as previously noted above. The examiner asserts that the system memory for containing the data references (CL5-L19-26) and simulated trace buffers (CL5-27), and the engine for generating data references to the cache simulator (CL5-L49) are inherent in the system disclosed by Blandy. Otherwise, the device would not operate.

Per dependent claim 24: As previously noted above, the data "identifiers" configured to identify memory segments would be necessarily inherent in the cache simulator disclosed by Blandy in order to track and identify real time trace and simulation data (see: Blandy CL5-L23).

Per dependent claim 25: Claim 25 merely identifies the simulated caches as consisting of segments 1 to M. The examiner again asserts that this feature is inherent in Blandy since it is necessary to identify (and assign) the simulated segments and caches as part of the cache simulation process.

Per dependent claim 26: As noted above, Blandy discloses applying the stored (collected) data references (i.e. the instruction cache and data cache accesses) to the cache simulator as inputs (CL5-L30). As also previously noted, the term "operational cache" is interpreted to simply be the modeled cache geometries used by the cache simulator in determining the cache performance on an operational data processing system and are hence equivalent to the trace data references of Blandy.

Per dependent claim 27: As noted above, Blandy teaches evaluating the performance in an information handling system (CL2-L21) that the examiner interprets to include a database management system.

Allowable Subject Matter

5. Claims 13-19 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a method and system for simulating the performance of a segmented cache memory of various sizes by applying data references to the simulated cache, storing the references in a trace buffer, calculating the number or "hits" or "misses" to the segments, and generating a performance estimate. This has been

disclosed in the prior art. The prior art of record, while generally disclosing these features, does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ***ipsissimis verbis*** *test, i.e., identity of terminology is not required.* ***In re Bond****, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

In particular, the prior art of record does not disclose the specific sequence of steps relating to and the arrangement of elements relating to generating an estimate of cache performance, via a multi-segmented cache simulator, using references received during operation of database management system, as required by independent claim 13.

The closest prior art uncovered during examination is:

- *U.S. Patent 5,940,618 issued to Blandy et al: discloses a cache simulator and performance evaluation as noted above.*
- *"Trace-Driven Memory Simulation: A Survey", R.A. Uhlig et al, ACM Computing Surveys, Vol. 29, No. 2, June 1997: discloses trace based cache simulation techniques and performance of commercially available cache simulators.*
- *"Automatic and Efficient Evaluation of Memory Hierarchies for Embedded Systems", S. Abraham et al, Hewlett-Packard # HPL-1999-132, October*

1999: discloses trace based cache simulation techniques and performance of the commercially available "Cheetah" simulator.

- *"Active Memory: A New Abstraction for Memory system Simulation", A.R. Lebeck et al, ACM Transactions on Modeling and Computer Simulation, Vol. 7, No. 1, January 1997: discloses fast-cache, trap-driven and trace based cache simulation techniques and performance of the commercially available simulators.*
- *"Retargetable Cache Simulation Using High Level Processor Models", R. Ravindran et al, IEEE 0-7695-0954-1/01, IEEE January 2001: discloses re-targetable cache simulation techniques and performance of the commercially available "Cheetah" simulator.*

These references generally disclose features relating to cache performance improvement using cache simulators. However, the prior art of record does not disclose specific sequence of steps and the arrangement of elements required by independent claim 13. Independent claim 13 includes limitations relating to storing references during operation of a data base management system, and maintaining a multi-segmented cache simulator with simulated buffers storing identifiers where the multiple caches include a set of segments that are different from the other caches. As noted above, the multi-segmented cache simulator is specifically defined by applicant's specification as multi-segments consisting of eight segments of cache simulator (200) that are designated as cache0-cache7 configured to hold 250,000 simulated buffers. (Specification page 9, lines 5-25, page 14, lines 12-27, and in Figs. 2 and 4a – 4b)

Claim 13 further includes limitations relating to the sequence of cache simulator steps for stored cache references including; searching a first buffer for referenced data item and, if in segmented memory increment first buffer hit counter & move reference to segment head, if not, increment miss counter & store identifier in second buffer, then store second buffer at head of cache simulator, and generate an estimate of performance. This specific sequence of steps for generating an estimate of cache performance, via a multi-segmented cache simulator, using references received during operation of database management system, is not explicitly disclosed in the prior art of record. Dependent claims 14-19 are allowable as being dependent from claim 13.

Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In this case, the prior art of record does not explicitly disclose the additional correction factor limitation of applying data references to the operational data cache to an initial miss rate in a second simulated cache, in multiple caches, where the number of buffers matches the number of buffers in the operational cache.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 5,910,900 issued to Mangelsdorf teaches cache simulation and optimization.

"Automatic and Efficient Evaluation of Memory Hierarchies for Embedded Systems", S. Abraham et al, Hewlett-Packard # HPL-1999-132, October 1999: discloses trace based cache simulation techniques and performance of the commercially available "Cheetah" simulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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